Listing of Claims

1. (Currently amended): A semiconductor process for controlling etching profile, comprising the steps of:

providing a plurality of substrates, ~~in which~~ wherein each substrate comprises a film to be etched and an overlying masking pattern layer ~~are provided overlying each substrate~~ thereon; and

etching ~~each of the films in sequence~~ the film to be etched on each substrate in a plasma chamber using the masking pattern layer as an etch mask, a polymer layer being deposited over the inner wall of the plasma chamber during the etching;

wherein an intermediary cleaning process is performed in the plasma chamber between the etchings before the deposited polymer layer reaches such a degree as to induce lateral etching on the ~~next~~ film to be etched of the next substrate.

2. (original): The semiconductor process of claim 1, wherein the film to be etched is a silicon layer.

3. (original): The semiconductor process of claim 2, wherein the intermediary cleaning process is performed before the deposited polymer layer leads to a spectral intensity associated with the layer to be etched from OES data analysis more than 100 at a wavelength about 405 nm.

4. (original): The semiconductor process of claim 1, wherein the mask layer is a silicon oxide layer.

5. (original): The semiconductor process of claim 1, wherein the intermediary cleaning process is performed between each of the etchings.

6. (original): The semiconductor process of claim 1, wherein the intermediary cleaning process is performed for 1~3 minutes.

7. (original): The semiconductor process of claim 6, wherein the intermediary cleaning further comprises the steps of:

using O_2, Cl_2, and SF_6 as a first cleaning gas for about 30 sec; and

using Cl_2, and HBr as a second cleaning gas for about 50 sec.

8. (original): The semiconductor process of claim 1, further comprising performing a preliminary cleaning process in the plasma chamber before placing the substrates therein.

9. (original): The semiconductor process of claim 8, wherein the preliminary cleaning process is performed for 8~12 minutes.

10. (original): The semiconductor process of claim 9, wherein the preliminary cleaning process further comprises the steps of:

using O_2, Cl_2, and SF_6 as a first cleaning gas for about 70 sec;

using O_2, Cl_2, and He as a second cleaning gas for about 200 sec;

using Cl_2, and HBr as a third cleaning gas for about 150 sec; and

using He as a fourth cleaning gas for about 30 sec.

11. (Previously presented): A method of forming floating gates for flash memory devices, comprising the steps of:

providing a plurality of substrates;

successively forming a floating gate dielectric layer and a polysilicon layer overlying each of the substrates;

forming a capping layer with a bird's beak overlying the polysilicon layer; and

etching each of the polysilicon layers in sequence in a plasma chamber using the overlying capping layer as an etch mask to form a floating gate on each of the floating gate dielectric layers, a polymer layer being deposited over the inner wall of the plasma chamber during the etching;

wherein an intermediary cleaning process is performed in the plasma chamber between the etchings before the deposited polymer layer reaches such a degree as to induce lateral etching on the next polysilicon layer.

12. (original): The method of claim 11, wherein the intermediary cleaning process is performed between each of the etchings.

13. (original): The method of claim 11, the intermediary cleaning process is performed for 1~3 minutes.

14. (original): The method of claim 13, wherein the intermediary cleaning process further comprises the steps of:

using O_2, Cl_2, and SF_6 as a first cleaning gas to perform the for about 30 sec; and

using Cl_2, and HBr as a second cleaning gas to perform the for about 50 sec.

15. (original): The method of claim 11, further comprising performing a preliminary cleaning process in the plasma chamber before placing the substrates therein.

16. (original): The method of claim 15, wherein the preliminary cleaning process is performed for 8~12 minutes.

17. (original): The method of claim 16, wherein the preliminary cleaning process further comprises the steps of:

using O_2, Cl_2, and SF_6 as a first cleaning gas for about 70 sec;

using O_2, Cl_2, and He as a second cleaning gas for about 200 sec;

using Cl_2, and HBr as a third cleaning gas for about 150 sec; and

using He as a fourth cleaning gas for about 30 sec.

18. (original): The method of claim 11, wherein the intermediary cleaning process is performed before the deposited polymer layer leads to a spectral intensity associated with the polysilicon layer from OES data analysis more than 100 at a wavelength about 405 nm.

19. (original): The method of claim 11, wherein the floating gate dielectric layer is a silicon oxide layer.

20. (original): The method of claim 11, wherein the capping layer is silicon oxide layer.

21. (original): A method of forming floating gates for flash memory devices, comprising the steps of:

providing a plurality of substrates;

successively forming a floating gate oxide layer and a polysilicon layer overlying each of the substrates;

forming a oxide layer with a bird's beak overlying the polysilicon layer; and

etching each of the polysilicon layers in sequence in a cleaned plasma chamber using the overlying oxide layer as an etch mask to form a floating gate on each of the floating gate oxide layers, a polymer layer being deposited over the inner wall of the plasma chamber during the etching;

wherein a cleaning process is performed in the plasma chamber between each of the etchings to remove the deposited polymer layer.

22. (original): The method of claim 21, wherein the cleaning process is performed for 1~3 minutes.

23. (original): The method of claim 22, wherein the cleaning process further comprises the steps of:

using O_2, Cl_2, and SF_6 as a first cleaning gas for about 30 sec; and

using Cl_2, and HBr as a second cleaning gas for about 50 sec.